IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An electronic device, comprising:

an accelerator for accelerating cryptographic data processing operations, which accelerator is arranged with:

a first logical interface over which data to be processed is provided, and

a secure second logical interface over which cryptographic keys employed in processing data is provided, wherein the first logical interface and the secure second logical interface share a same physical interface, and

a configuration register arranged to indicate to the accelerator whether secure mode or normal mode is set by a processor, and configured to receive mode setting instructions from a protected application, said processor arranged in the device.

2. (Cancelled).

3. (Cancelled)

4. (Previously Presented) The device according to claim 1, wherein the configuration register further is arranged such that it may be set in one of a plurality of possible encryption modes, the accelerator being arranged to operate in the encryption mode set in the register.

5. (Previously Presented) The device according to claim 1, wherein the accelerator is arranged such that the first logical interface and the secure second logical interface are provided via respective physical interfaces.

6. (Previously Presented) The device according to claim 1, wherein the first logical interface of the accelerator is arranged such that it is accessible by any application, while the secure second logical interface of the accelerator is arranged such that it is accessible by protected applications only.

7. (Previously Presented) The device according to claim 6, further being arranged such that protected applications may prevent other applications from accessing the accelerator.

8. (Previously Presented) The device according to claim 6, wherein protected applications are applications which are allowed to execute in the secure execution environment.

9. (Previously Presented) The device according to claim 1, further comprising:

storage circuitry arranged with at least one storage area in which protected data relating to device security are located, and wherein

a processor is arranged such that it may be set in one of at least two different operating modes; and, the device being further arranged such that:

the processor is given access to said storage area, in which said protected data are located, when a secure processor operating mode is set,

the processor is denied access to said storage area when a normal processor operating mode is set; and

the processor is capable of accessing the secure second logical interface of the accelerator, when the secure processor operating mode is set.

10. (Previously Presented) The device according to claim 9, wherein the processor further is arranged such that protected applications control the processor operation mode.

11. (Previously Presented) A mobile communication terminal comprising a device according to claim 1.

12. (Currently Amended) A device for acceleration of data processing operations, which device comprises:

a first logical interface over which data to be processed is provided; and

a secure second logical interface over which cryptographic keys employed in processing said data is provided, wherein the first logical interface and the secure second logical interface share a same physical interface, and

a configuration registered arranged to indicate to the device whether secure mode or normal mode is set by a processor, and configured to receive mode setting instructions from a protected application, said processor being arranged in the device.

13. (CANCELLED)

14. (CANCELLED)